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SADRŽAJ

A Realisation of Synchronous Buck Power Converter for Energy Harvesting from Vibrations

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***Abstract*— The paper presents the implementation of a synchronous "buck" power converter that is used to energy harvesting from vibrating structures that oscillate in the 1Hz-1kHz range. This range is the most common in real cases. In addition to the frequency, a very important parameter is also the amplitude of the vibrations. Usually, low frequencies (< 10Hz) are associated with larger oscillatory masses and larger oscillation amplitudes, while higher frequencies (1kHz >f > 100Hz) refer to larger oscillatory masses and smaller oscillation amplitudes. The realized power converter is based on the integrated circuit LT3588-1, in which it integrates a low-loss full-wave bridge rectifier with a high efficiency synchronous "buck" converter to form a complete energy harvesting solution optimized for high output impedance of mechanic/electric converter such as piezoelectric lead zirconate titanate (PZT) ceramics or polymer based on polyvinylidene fluoride (PVDF), or other composite. The paper presents experimental results obtained on the vibration platform as vibration source, in order to testing of the proposed power converter in laboratory conditions.**

Keywords—power converter, synchronous buck, vibrations, energy harvesting, PZT, PVDF

I. INTRODUCTION

Energy harvesting from mechanical vibration structures by means of various types of piezoelectric elements can provide energy for low power electronic devices such as microcontrollers with low power consumption, data loggers, wireless sensors, etc. [1-3]. However, the generated instantaneous mechanical power originating from the vibrating structure is usually pulsed or quasi-harmonic, it is also unstable, and is obtained with a relatively low efficiency of converting mechanical to electrical energy. Vibrations are especially present in transport and industrial machines. Different form of electromechanical devices can be used as energy harvester on the mechanical structures that oscillate or vibrate.

The most commonly used energy harvesters are electromagnetic (consisting of an electromagnetic coil and a core), electrostatic which are based on the change of capacitance and piezoelectric which are made of piezo ceramics and which use the piezoelectric effect during the deformation of the corresponding material. This devices are based PZT or PVDF. Usually, the deformation is realized in the longitudinal or transverse direction [4]. Ceramic piezoelectric elements exhibit a piezoelectric effect when the crystal structure of the ceramic is compressed and internal dipole movement produces a voltage. Polymer elements comprised of long-chain molecules produce a voltage when flexed as molecules repel each other. Ceramics are often used under direct pressure while a polymer can be flexed more readily.

Fig. 1 shows the power density for three different types of vibrating energy harvesters. It is seen that piezo's performs better at "high" frequencies (> 100Hz) and electromagnetic are best at low frequencies (< 100Hz) [3].

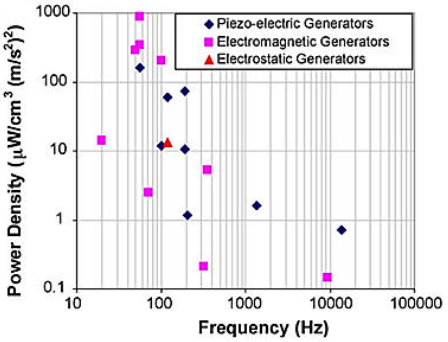

Fig. 1. Power density for three types of vibrating energy harvester depending on the frequency [3].

The number of scientific papers dedicated to piezoelectric energy harvesting is abruptly growing. Main problem is high toxicity of lead based materials (since the most efficient piezoelectric energy harvesters are lead based) and low efficiency of lead-free harvesters developed until now. The idea of the many inventions [5-7] is to use newly examined materials for this purpose and to implement them in our surroundings where they will harvest the energy without negative impact on environment and human health. Companies SCIOCS and PANASONIC developed (K, Na)NbO3 lead-free material for energy harvesting but this kind of films are made on rigid substrates without the possibility to conform to different shapes and surfaces.

There are also some companies as PolyK, USA that use this kind of polymer for harvesting purpose, but they use expensive electrically active PVDF copolymers. In the investigations presented in [8-9], the low cost electrically non- active alpha phase PVDF was used and with the application of poling system it turned into electrically active one (beta and gamma). Poling is necessary for the orientation of ferroelectric domains in ceramic component, but it positively affects the reorientation of polymer chains of PVDF. Combining these two characteristics enables the formation of low cost and eco-friendly energy harvester for everyday use. Another advantage of the polymer matrix is the prevention of the corrosive effects of the environment on the piezoelectric component, extending the lifetime of the material.

The basic schematic diagram of the system for harvesting and converting mechanical vibration energy into electricity is given in Figure 2. The system consists of the following blocks: (1) mechanical vibration source, (2) piezoelectric (PZT) or polymer PVDF, mechanical to electrical converter,

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(3) rectifier with capacitor for temporary energy storage and voltage limiter (Zener diode), (4) switching voltage regulator (DC/DC converter) and (5) battery bank (or super capacitor) from which some DC load can be supplied.

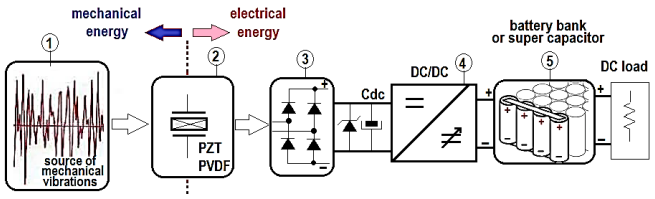

Fig. 2. Basic block diagram of energy harvesting and power conversion form vibration to electrical energy.

The generator of vibrations or mechanical shocks produces a force with a stochastic amplitude in a certain range or with a fixed value depending on the specificity of the mechanical energy source (1). This force is then transformed into electrical energy by means of a mechanical/electrical converter (2) which can be piezoelectric PZT based on ceramics or PVDF based on composite polymers. It is necessary to provide enough energy to feed the load in a given period of time so that the energy is temporarily stored in the capacitor that is charged via the diode rectifier (3). The DC link voltage is then converted via a DC/DC power converter (4) to the required value voltage determined by the battery bank (5) and the DC load current.

Several types of power converter topologies in the energy harvesting system can be found in the literature. In this part, a brief overview of them will be given. The most commonly used circuit is called classic interface. This circuit consist of a diode rectifier, filter capacitor and load. The disadvantage to this circuit is that the current flowing to the load is discontinuous and the vibratory velocity is not in phase with the piezoelectric voltage. Therefore this circuit won't work in an efficient way.

As it was said this circuit is only a standard circuit which will not increase the energy therefore the series and parallel synchronized switch harvesting (SSHI) and synchronized electric charge extraction (SECE) have been suggested to for increasing the power[3],[10]. Voltage doubler circuit [10] is very similar to the classic full bridge circuit. As its name suggests, this circuit is a voltage multiplier circuit that can increase the output voltage by a factor of two. This circuit is practical for some application when electric load with high resistance needs high power, like TV and radio devices [10]. The integrated circuit (IC) named LTC3588-1 integrates a low-loss full-wave bridge rectifier with a high efficiency buck converter to form a complete energy harvesting solution optimized for high output impedance energy sources such as piezoelectric PZT or PVDF[11].

In this paper is presented one possible application of this IC in the power conversion system for energy harvesting from vibratory and impact structure.

II. Description of Experimental Prototype

This chapter describes the realized experimental set-up in order to application the "buck" DC/DC power converter for the conversion of vibration and shock pulses into a constant DC voltage for supplying a low-power load (wireless sensor power supply). The solution is based on the LTC3588-1 integrated circuit (IC) [11].

The topology used in this case is based on the principle scheme shown in Fig.2, while the electrical diagram of the realized energy harvester and DC/DC power converter are given in Fig.3. Within the integrated circuit LTC3588-1 there are a full-wave diode bridge with low losses and a high-frequency high efficiency synchronous buck DC/DC power converter.

In this way, a complete energy harvesting solution optimized for mechanical energy harvesters, such as piezoelectric PZT modules based on ceramics or PVDF based on composite thin polymer films, was realized.

The IC LTC3588-1 has an ultra-low quiescent current in under voltage lockout (UVLO) mode and a relatively wide hysteresis range allows charge to accumulate on an input capacitors C1 and C2 until the buck converter can efficiently transfer a portion of the stored charge to the output. The capacitor C1 is ceramics type, while C2 is electrolyte.

The IC provides four DC output voltage values that can be selected via the appropriate selector switches. Possible output voltage values are: 1.8V, 2.5V, 3.3V and 3.6V, with a maximum output current of 100mA. Particularly interesting for practical applications are voltages 3.3V and 3.6V.

The output capacitor may be sized to service a higher output current burst. An input protective shunt set at 20V (i.e. Zener diode) enables greater energy storage for a given amount of input capacitance C2. Rectified voltage on capacitors C1, C2 (pin 4-V_{in}) which are used as an energy storage for the synchronous voltage regulator. The diode rectifier at the inputs PZ1, PZ2 has a total voltage drop of about 400mV at a typical current value of 10µA generated by PZT or PVDF modules. The maximal output current of the diode rectifier is about 50mA.

Two internal rails, CAP and VIN2, are used to correct drive the high side PMOS and low side NMOS of the "buck" power converter, respectively. Additionally the VIN2 rail serves as logic high level for output voltage select bits D0 and D1. In this concrete case 3.6V output voltage is selected when is D0 and D1 are equal "logic 1". Also this two bits determine UVLO threshold for VIN. This voltage rising at threshold typically 5V (4.73Vmin and 5.37Vmax) and falling at threshold 4V (3.73Vmin and 4.03Vmax).

The VIN2 rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below VIN. Bypass capacitors C3, C4 are connected to the CAP and VIN2 pins respectively, to serve as energy reservoirs for driving the buck switches PMOS/NMOS. When VIN is below 4.8V, VIN2 is equal to VIN and CAP is held at GND. In manual [11] is show the graphical presentation for optimal VIN, VIN2 and CAP relationship.

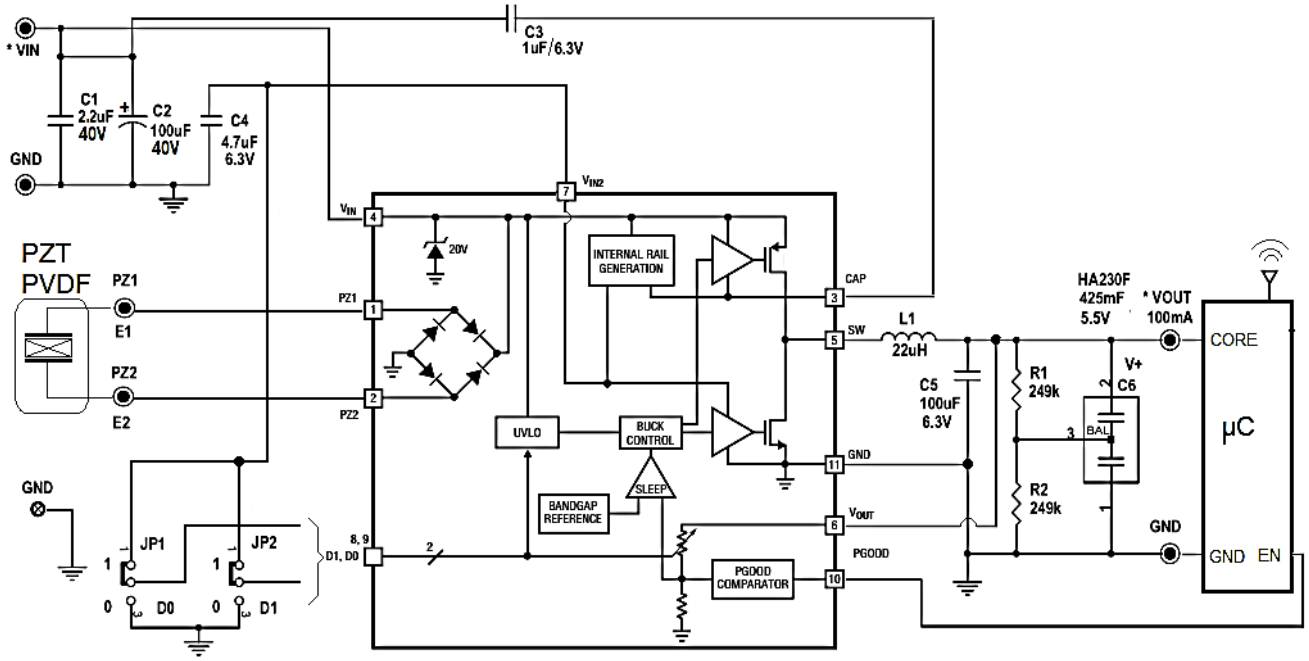

Fig. 3. Electric diagram of the implemented piezoelectric energy harvester based on a "synchronous buck" DC/DC power converter.

The synchronous buck DC/DC power converter is based on PI hysteresis voltage control using internal feedback on the output voltage V_{out}, as shown in Fig.4.

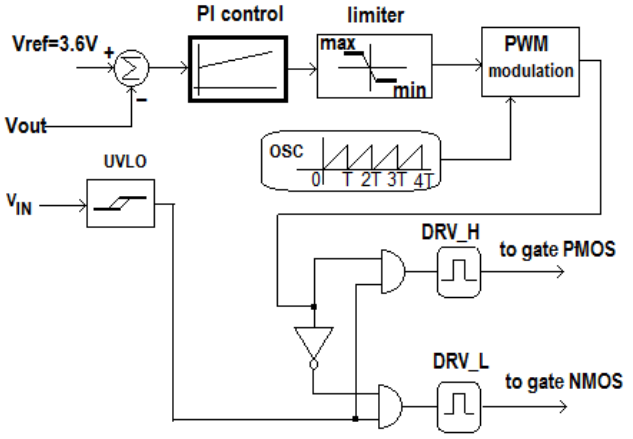

Fig. 4. Principal control block diagram of synchronous "buck" power converter.

In this particular case, the reference value of the output voltage V_{ref} =3.6V is set. The synchronous buck charges the output capacitor via choke L1 to a value slightly higher than the level of the set voltage at the output. This is provided by increasing the current of the choke L1 to a maximum value (typically 260mA) via an internal PMOS switch and then decreasing the current from the maximum value to a zero value (i.e. 0mA), via an internal NMOS switch (see Fig.3). In this way, energy is efficiently delivered to the output capacitors (C5 and C6).

The duration of the rise rate is determined by the values of V_{in}, V_{out} and the value of the inductance L1. If the input voltage falls below the drop threshold UVLO before the output voltage reaches the set value, appropriate logic is activated within the control circuit to blocking the drive pulses on the gates PMOS and NMOS semiconductor switches. In this way the "buck" power converter will turn off and will not turn on until the input voltage Vin rises above the threshold UVLO again.

The synchronous "buck" power converter is optimized to work with an inductor in the range of 10µH to 30µH, although inductor values outside this range may yield benefits in some applications. A larger inductor will benefit high voltage applications by increasing the on-time of the PMOS switch and improving efficiency by reducing gate charge loss. In this application is choose an inductor 22µH with a maximum DC current rating of 100mA. The DC resistance (DCR) of the inductor can have an impact on efficiency as it is a source of loss.

A so called *"power good comparator"* [11] produces a logic high referenced to VOUT on the PGOOD pin the first time the converter reaches the sleep threshold of the programmed VOUT, signalling that the output is in regulation. The PGOOD pin will remain high until VOUT falls to 92% of the desired regulation voltage. Several sleep cycles may occur during this time. Additionally, if PGOOD is high and VIN falls below the UVLO falling threshold, PGOOD will remain high until VOUT falls to 92% of the desired regulation point. This allows output energy to be used even if the input is lost.

The input and output capacitors were select based on the energy needs and load requirements of the application. In every case the capacitor connected to pin VIN should be selected to withstand the highest voltage present at VIN. For load current of 100mA or smaller, storing energy at the input capacitor takes advantage of the high voltage input since the buck can deliver 100mA average load current efficiently to the output. The input capacitor is sizing to store enough energy to provide maximal output power for the load time duration which is required. Enough energy should be stored on the input so that the synchronous "buck" power converter does not reach the UVLO falling threshold which would halt energy transfer to the output. The basic relation which is used to designing input capacitor is:

$$W_{in} = \frac{P_{load} \cdot t_{load}}{\eta} = \frac{1}{2} \cdot C_{in} (V_{in}^2 - V_{UVLO\_fall}^2) \quad (1)$$

This equation may overestimate the input capacitor necessary since load current can deplete the output capacitor all the way to the lower PGOOD threshold. It also assumes

that the input source charging has a negligible effect during this time. In equation (1) η is the efficiency for the maximum of load power of the synchronous "buck" converter and Vin is the input voltage when the "buck" begins to switch. In this design it is assumed that is η=0.95 (for maximal load power). For load 3.6V/100mA i.e. P_{load}=0.36W, load time of 1ms, V_{in}=5.2V and UVLO falling threshold of 4V the calculation value of the input capacitor of C2=72μF was obtained. The first higher standard value is adopted C^*2=100μF. Based on maximum value of input voltage 30V from PVDF module and previously calculation a 100μF/40V input capacitor was selected.

The duration for which the "buck" regulator sleeps depends on the load current and the size of the output capacitor. The DC sleep hysteresis window is ΔH= ±12mV around the programmed output voltage V_{out}. The sleep time T_s is determined by the following equation:

$$T_s = \frac{\Delta H(+) - \Delta H(-)}{I_{load}} \cdot C_{out} \qquad (2)$$

In regulation, the LTC3588-1 enters a sleep state in which both input and output quiescent currents are minimal. The buck converter turns on and off as needed to maintain regulation. For accepted sleep time approximately 25μs, and for load current of 100mA, ΔH (+) – ΔH (-) =12mV-(-12mV) =24mV the calculation value of the output capacitor of C5 =100μF was obtained. For the rated output voltage 3.6V, a 100μF/6.3V capacitor C5 was selected.

At the output, in parallel with the electrolytic capacitor C5 of the synchronous "buck" converter, a super capacitor can optionally be placed. In this particular case, the super capacitor HA230F/425mF/5.5Vdc was chosen with the corresponding resistive divider R1-R2 (R1=R2=249k, 1/16W, 1%, which can ensure the stability of the power supply of the load at the output of the "buck" converter (the load is a microcontroller as part of a wireless sensor network). Supercapacitor is particularly useful for increased output energy storage and battery backup applications.

III. Experimental Results

This chapter presents the experimental results obtained during operational testing of the implemented energy harvesting power converter (a synchronous "buck" voltage i.e. step-down converter) with the electrical scheme of which is shown in Fig.3. This power conversion module is used in combination with polymer PVDF mechanical energy harvester device. The polymer PVDF electromechanical module is realized as a sandwich configuration of multiple integrated individual PVDF cells, and its output voltage is 30Vmax at an output electric power of about 1W. The presented results refer to several types of oscillatory mechanical excitation, frequency range 1Hz-1kHz, which were used during the experiments. Testing of the PVDF modules in the above mentioned frequency range was performed on a mechanical hydraulic vibration platform, which is described in detail in the references [12-13]. The electrical measurements were made on a four-channel digital memory oscilloscope GW INSTEK, type MDO-2204EX, 200MHz, 1Gs/s. In the experiments, the following quantities were measured and displayed on oscilloscope images: the voltage output of the PVDF element (proportional to the mechanical acceleration), the voltage at the input terminals PZ1-PZ2 of the LTC3588-1 integrated circuit, the voltage V_{in} at the input capacitor C2 and the output voltage V_{out} at the load. The experimental results are obtained for output capacitor C5=100μF.

A. Experiment 1

In this experiment, a mechanical impulse excitation of the PVDF sandwich with a frequency of 1Hz was set. For the case of sinusoidal oscillatory excitation with a frequency of 1Hz, the formed PVDF sandwich does not have a significant value of voltage and current, so in this part the experimental results for impulse excitation are given. Fig.5 shows the obtaining characteristic waveforms recorded on an oscilloscope. For the maximum excitation voltage 30V of the PVDF module, the voltage on the input capacitor C2 was 19V, and its peak-to-peak ripple was about 250mV. Under these conditions and with a load current of 5mA, the output voltage was V_{out}=3.6V. The current value of load current specified in experiment is the maximum value that can be achieved. The voltage at the terminals PZ1-PZ2 is limited to ±20V, which is a consequence of the use of a Zener diode connected in parallel with the capacitor C2 in the DC-link circuit (see electrical scheme on Fig.3).

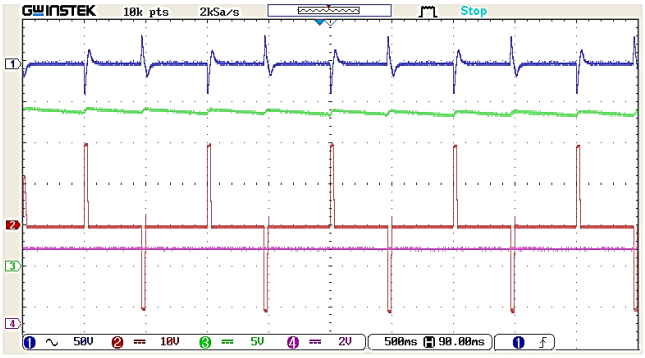

Fig. 5. The characteristic waveforms for pulse excitation frequency of 1Hz; CH1- PVDF output voltage (50V/div), CH2-voltage at terminal PZ1-PZ2, (10V/div), CH3- input DC voltage V_{in} (5V/div), CH4-output voltage V_{out} (2V/div), Time (500ms/div).

B. Experiment 2

In this experiment, a quasi-sinusoidal (THD≈10%) mechanical excitation of the PVDF sandwich with a frequency of 10Hz was applied. The recorded waveforms are shown in Fig.6.

The PVDF voltage was amount $30V_{max}$. The voltage on the input capacitor was 20V, while its ripple was less than 10mV. The voltage at the terminals PZ1-PZ2 is limited to ±20V (approximately a trapezoidal waveform). The output voltage was V_{out}=3.6V at a load current of 30mA.

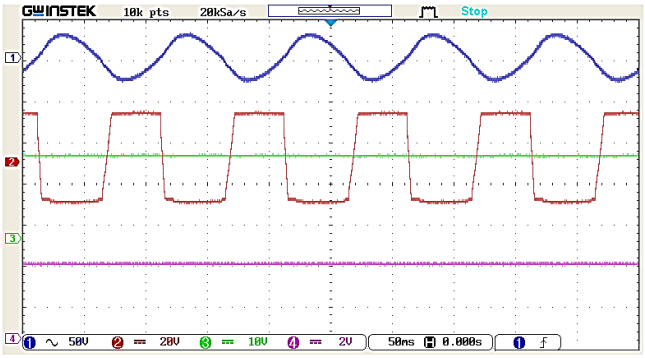

Fig. 6. The characteristic waveforms for quasi sinusoidal excitation frequency of 10Hz; CH1- PVDF output voltage (50V/div), CH2-voltage at terminal PZ1-PZ2, (20V/div), CH3- input DC voltage V_{in} (10V/div), CH4-output voltage V_{out} (2V/div), Time (50ms/div).

C. *Experiment 3*

In this experiment, a pure sine mechanical excitation of the PVDF sandwich with a frequency of 100Hz was applied. The recorded waveforms are shown in Fig.7.

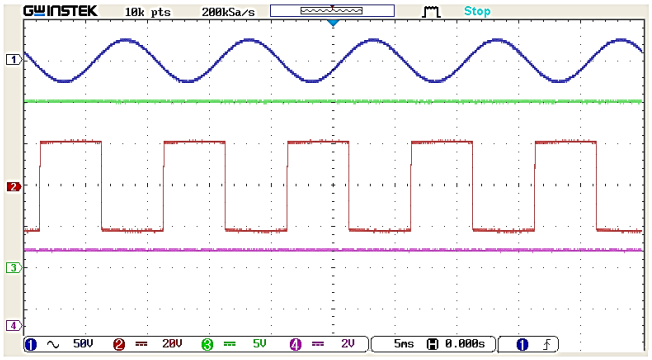

Fig. 7. The characteristic waveforms for sinusoidal excitation frequency of 100Hz; CH1- PVDF output voltage (50V/div), CH2-voltage at terminal PZ1-PZ2, (20V/div), CH3- input DC voltage V_{in} (5V/div), CH4-output voltage V_{out} (2V/div), Time (5ms/div).

The PVDF voltage was amount $30V_{max}$. The voltage on the input capacitor was 20V, while its ripple was less than 10mV. The voltage at the terminals PZ1-PZ2 is limited to ±20V (pure a square waveform). The output voltage was V_{out}=3.6V at a load current of 50mA.

D. *Experiment 4*

In this experiment, a pure sine mechanical excitation of the PVDF sandwich with a frequency of 1kHz was applied. The recorded waveforms are shown in Fig.8. The PVDF voltage was amount 30Vmax. The voltage on the input capacitor was 20V, while its ripple was less than 10mV. The voltage at the terminals PZ1-PZ2 is limited to ±20V (pure a square waveform). The output voltage was V_{out}=3.6V at a load current of 100mA.

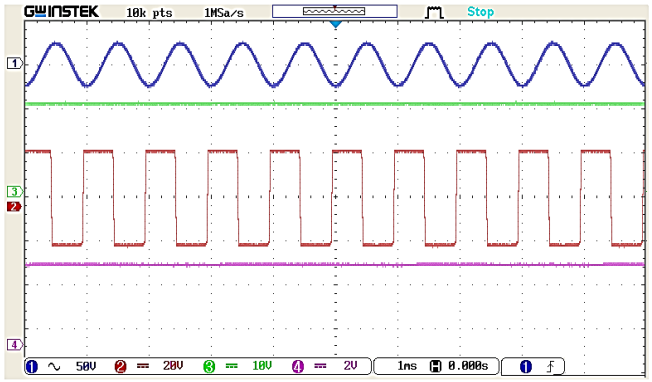

Fig. 8. The characteristic waveforms for sinusoidal excitation frequency of 1kHz; CH1- PVDF output voltage (50V/div), CH2-voltage at terminal PZ1-PZ2, (20V/div), CH3- input DC voltage V_{in} (5V/div), CH4-output voltage V_{out} (2V/div), Time (1ms/div).

E. *Experiment 5*

This experiment was performed at an excitation frequency of 100Hz with maximal value of the PVDF voltage of 30V and an output current overload of 20% relate to rated value. In effect, the actual load was set so that its current was 120mA (i.e. 20% overload). Under these conditions, it is possible to verify the operation of the system in the UVLO mode based on the obtained waveforms. Fig.9 shows that under these conditions the ripple of the input voltage is significant, and therefore so is the ripple of the output voltage. The input voltage ripple is due to overload. The average value of input voltage V_{in} was amount 5V. The input voltage ripple was about 1V (i.e. 20%). The average value of the output voltage was 1.6V and its voltage ripple was 1.2V (i.e.75%). In overload conditions, there is a significant drop in the output voltage and the appearance of a relatively large ripple. The voltage at the input terminals PZ1-PZ2 is a rectangular voltage with a pronounced envelope, which is a consequence of the input voltage ripple.

In this regime and from the oscilloscope recordings, the characteristic voltage thresholds for the LTC3588-1 circuit can be clearly observed.

For the input voltage lower than the voltage threshold $V_{in}(+)$ =5.2V, the output voltage tends to decrease. When the input voltage reaches 5.2V, the output voltage increases from 0.8V. This voltage increases to the value of 1.6V voltage, that is, until the moment when the input voltage drops to the value of the voltage threshold $V_{in}(-)$ = 4V. The measured voltage thresholds of the input voltage correspond to the technical characteristics of the integrated circuit LTC3588-1.

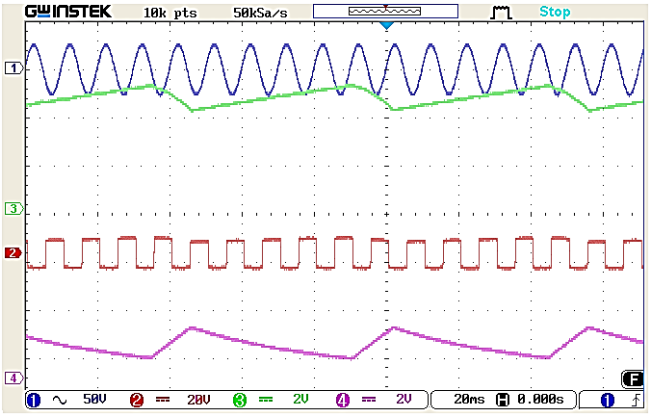

Fig. 9. The characteristic waveforms for sinusoidal excitation frequency of 100Hz and output current of 120mA; CH1- PVDF output voltage (50V/div), CH2-voltage at terminal PZ1-PZ2, (20V/div), CH3- input DC voltage V_{in} (5V/div), CH4-output voltage V_{out} (2V/div), Time (20ms/div).

The recorded mode in this experiment has no major practical significance, but it was used to verify the UVLO voltage thresholds and their influence on the output voltage.

IV. CONCLUSION

The paper gives a certain overview and problems within the scope of the key research so far related to energy harvesting from mechanical vibrations and vibratory structures. As part of the research on the synthesis of new PZT and PVDF materials as energy harvesters, this paper presents a possible solution of the switching topology of the power converter for collecting mechanical vibration energy and its conversion into electrical energy, using piezoelectric modules as primary mechanical/electrical sources. Special emphasis is given to the topology of the energy harvester based on the synchronous DC/DC voltage step-down power converter (i.e. "synchronous buck") with output characteristics of 3.6V/100mA. The load of the realized power converter is a microcontroller that is part of a wireless sensor network. The paper also provides a calculation of input and output capacitors of the proposed power converter

in accordance with the technical requirements for the load and the characteristics of the integrated circuit LT3588-1. Experimental results and measurements for a relatively wide frequency range of mechanical vibrations 1Hz -1 kHz were performed on the realized power converter, and integrated PVDF modules in one compact PVDF sandwich with an output power of about 1W were used as mechanical/electrical source. Finally, a detailed presentation and analysis of the key experimental results are given.

This paper presents some initial and relatively crude initial results related to voltage conversion from a one type of PVDF module and obtaining a stable voltage of 3.6Vdc for the load current 100mA that could have potential applications for powering sensors or autonomously powering low-power systems exposed to vibrations.

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